WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

a gate line formed on the substrate;

a plurality of storage conductors formed on the substrate, each storage conductor including a plurality of branches;

a gate insulating layer formed on the gate line and the storage conductor;

a semiconductor layer formed on the gate insulating layer;

a data conductor formed on the semiconductor layer;

a passivation layer formed on the data conductor; and

a pixel electrode formed on the passivation layer,

wherein at most one of the branches of each storage conductor has an isolated end.

2. The thin film transistor array panel of claim 1, wherein adjacent two of the storage conductors have at least two connections.

3. The thin film transistor array panel of claim 1, further comprising a connection bridge connecting adjacent two of the storage conductors across the gate line.

4. The thin film transistor array panel of claim 1, wherein each storage conductor comprises two longitudinal branches and two oblique branches, and the branches of each storage conductor form a closed loop.

5. The thin film transistor array panel of claim 1, wherein each storage conductor comprises two longitudinal branches and three oblique branches, and the branches of each storage conductor form two closed loops.

6. The thin film transistor array panel of claim 1, wherein each storage conductor comprises two longitudinal branches and four oblique branches, and the branches of each storage conductor form three closed loops.

7. The thin film transistor array panel of claim 1, wherein the pixel electrode has a plurality of cutouts, and at least one of the cutouts overlaps the storage conductors.

8. The thin film transistor array panel of claim 1, wherein the data conductor has substantially the same planar shape as the semiconductor layer except for a channel portion of the semiconductor layer.